Consider a hypothetical microprocessor generating a 16-bit address (for example, assume that the program counter and the address registers are 16 bits wide) and having a 16-bit data bus.

**What** is the maximum memory address space that the processor can access directly if it is connected to a “16-bit memory”?

Maximum memory address space is 64Kbytes (2^16).

**What** is the maximum memory address space that the processor can access directly if it is connected to an “8-bit memory”?

Answer with Explanation

The largest possible memory address space is 64Kbytes, or 216. Therefore, in (a) and (b), the microprocessor must access 64K bytes; however, the access to an 8-bit memory will only transfer an 8-bit word, but an access to a 16-bit memory may only transfer an 8-bit or 16-bit word.

**What** architectural features will allow this microprocessor to access a separate “I/O space”?

Answer with Explanation

Because it will generate different I/O signals during execution, separate I/O instructions are required. These signals won't be the same as the memory signals produced when memory instructions are executed. As a result, one more output pin will be required for I/O signals.

If an input and an output instruction can specify an 8-bit I/O port number, how many 8-bit I/O ports can the microprocessor support? **How** many 16-bit I/O ports?

**Answer with Explanation:**

The CPU can support 2 ^8 = 2568-bit input ports and 2 ^8 = 256 8-bit output ports with an 8-bit I/O port number. The microprocessor can support 2 ^8 = 256 16-bit input ports and 2 ^8 = 256 16-bit output ports with an 8-bit I/O port number.

Because the number of I/O ports depends on the number of bits used to encode the I/O port number, changing the size of the I/O port will not change the number of I/O ports (equals to8 bitsin both cases)